APPLICATION NOTE

AN220

Synchronizing and clock driving solutions – using the 74F50XXX family

1989 Sep

Philips
Semiconductors

PHILIPS

Synchronizing and clock driving solutions – using the 74F50XXX family

AN220

THE 74F50XXX FAMILY

- 74F5074 synchronizing dual D-type flip-flop
- 74F50728 synchronizing cascaded D-type flip-flop
- 74F50729 synchronizing dual D-type flip-flop with edge-triggered set and reset
- 74F50109 synchronizing dual J-$\overline{K}$ positive edge-triggered flip-flop

MAJOR FAMILY FEATURES

- Metastable immune characteristics
- Propagation delay skew and output to output skew guaranteed to be less than 1.5ns
- Balanced output currents for clock driver applications ($I_{OH} = I_{OL} = 20mA$)

INTRODUCTION

The Philips Semiconductors 74F50XXX series of products have been designed to resolve synchronization problems and at the same time produce complementary metastable/immune outputs with remarkably small skews useful in clock driving applications. The 74F5074 and 74F50109 are pin and function compatible replacements of the 74F74 and 74F109 respectively. The 74F50728 consists of two pair of cascaded D-type flip-flops, and the 74F50729 is a pin compatible replacement for the 74F74 with edge-triggered set and reset inputs.

SYNCHRONIZATION

Synchronizing incoming signals to a system clock has proven to be costly, either in terms of time delays or hardware. In order to synchronize a signal, a flip-flop is normally used to 'capture' the incoming signal. When a flip-flop is used in this mode, its setup and hold times are occasionally violated. Whenever this occurs, the flip-flop can enter a metastable state causing the outputs to glitch, oscillate, enter an intermediate state or change state in some abnormal fashion. Any of these conditions could cause a system to crash. To minimize this risk, flip-flops are often cascaded so that the input signal is captured on the first clock pulse and released on the second clock pulse (see Figure 1). This gives the first flip-flop about one clock period minus its propagation delay and minus the second flip-flop's clock-to-Q setup time to resolve any metastable condition. This method greatly reduces the probability that the outputs of the synchronizing device may display an abnormal state, but the trade-off is that one clock cycle is lost to synchronize the incoming signal. Often two separate flip-flop packages are required to produce the cascaded flip-flop circuit.

The 74F50XXX series of products have five design features that cause them to be immune from metastability problems. First, the flip-flops are designed so that their outputs cannot change state until any internal metastability has been resolved. This assures that the outputs will not glitch, oscillate, enter an intermediate state, or change state in some abnormal fashion. Second, the setup and hold time window has been minimized to reduce the likelihood of internal flip-flops entering a metastable state. Third, the internal flip-flops have specifically been designed to exit a metastable state as rapidly as possible. Fourth, the Clock-to-Q propagation delays through the part have been made as short as possible. Finally, Philips Semiconductors has used the best oxide-isolated process available to make these products the best synchronization solutions possible.

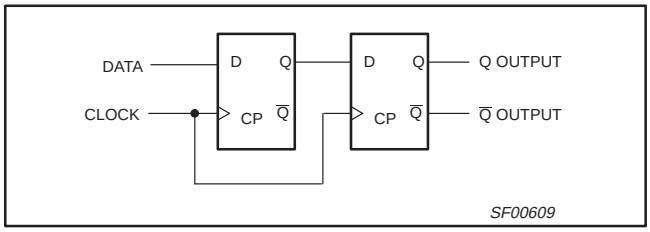

Figure 1. Cascaded Flip-Flops

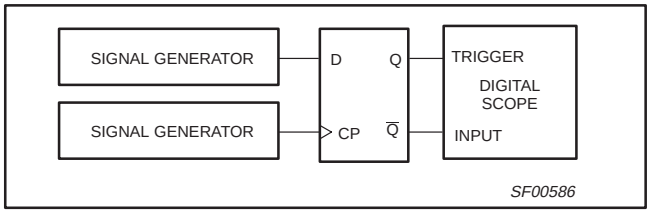

Figure 2. Test Setup

METASTABLE IMMUNITY

Philips Semiconductors uses the term 'metastable immune' to describe characteristics of some of the products in its FAST family, specifically the 74F50XXX family which presently consists of 4 products. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 74F5074.

When a test is performed (see Figure 2) where two independent signal generators are running at nearly the same frequency (in this case 10MHz clock and 10.02MHz data) the device-under-test operates continuously in the region where metastability can occur. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform.

When the device-under-test is a 74F74 (which was not designed with metastable immune characteristics) the waveform appears as shown in Figure 3. This figure clearly shows that the Q output can vary in time with respect to the Q trigger point. It also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a micro-channel plate CRT. Perhaps of even greater interest are the dots running along the 3.5 volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state, even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

When the device-under-test is a metastable immune part, such as the 74F5074, the waveform appears as shown in Figure 4. The 74F5074 $\overline{Q}$ output does not vary with respect to the Q trigger point even when the part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Semiconductors patented circuitry. If a metastable event occurs within the flip-flop the only outward manifestation of the event will be an increased Clock-to-Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the device (see below).

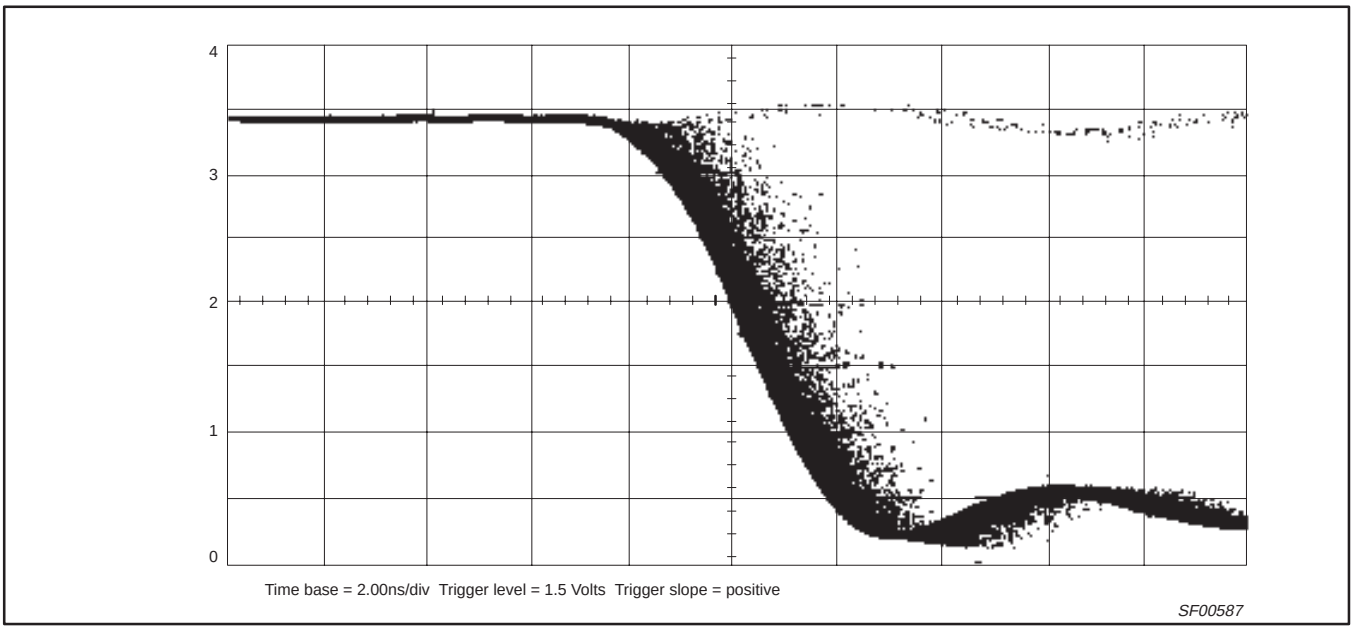

Figure 3. 74F74 $\overline{Q}$ Output Triggered by Q Output, Setup and Hold Times Violated

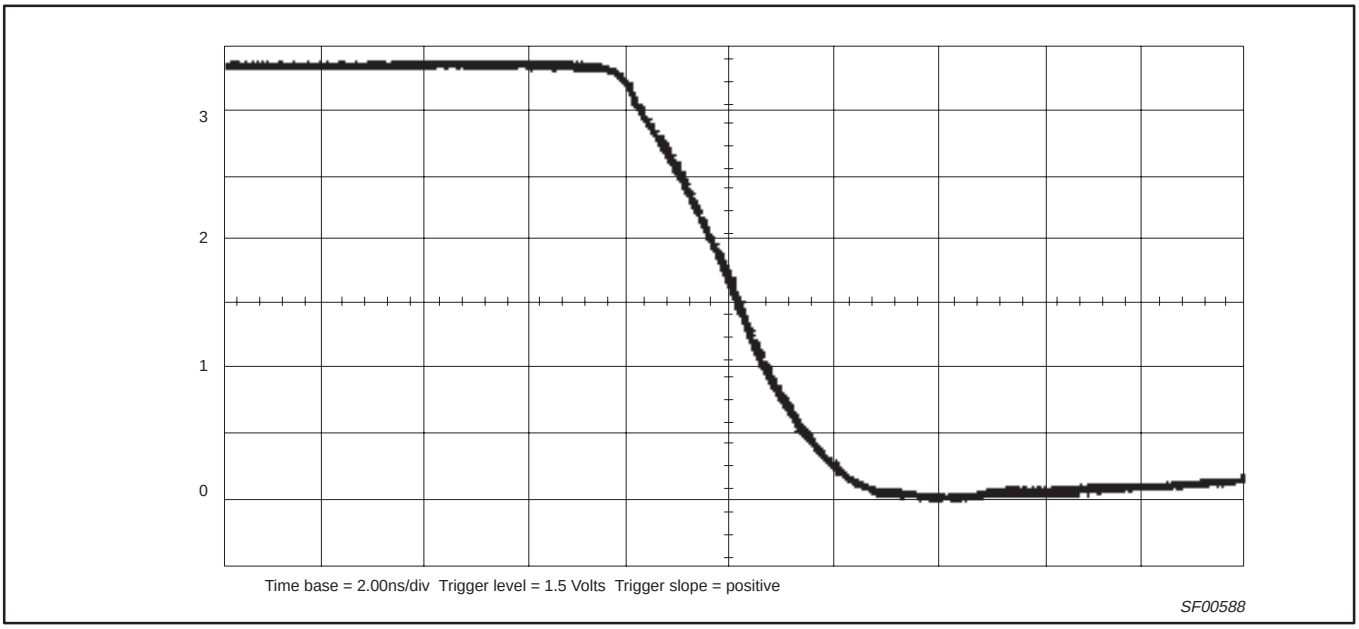

Figure 4. 74F5074 $\overline{Q}$ Output Triggered by Q Output, Setup and Hold Times Violated

METASTABILITY CHARACTERISTICS

In order to define the metastability characteristics of these products, Philips Semiconductors has chosen to use the parameters described by Thomas J. Chaney and Fred U. Rosenberger of Washington University in St. Louis, Missouri in their paper "Characterization and Scaling of MOS Flip-flop Performance in Synchronous Applications" in the *Proceedings of the Caltech Conference on VLSI*, January 1979. These parameters were chosen because they are fundamental and the best papers written on metastability use these parameters.

The first parameter to be considered is T_0. T_0 is a function of the propensity of a latch to enter a metastable state. It is also a very strong function of the normal propagation delay of the device and is generally given in units of seconds. The second parameter is h. It is the propagation delay from Clock-to-Q through a device under normal (i.e., no internal metastability) operation. The final parameter is tau (τ). Tau is the exponential time constant of the rate at which a latch in a metastable state resolves that condition and is typically specified in tenths of nanoseconds. Tau is generally the most important of the defining parameters.

To determine the Mean Time Between Failures (MTBF), the following formula is used:

$$MTBF = \frac{\left[\exp\left(\frac{t'}{\tau}\right)\right]}{\left[T_0(\text{clock rate})\ (\text{input data rate})\right]}$$

where t′ is the time given between the flip-flop clock and the output sampling time. This time is always greater than h. One point to keep in mind is that the input data rate is twice the frequency of the input signal because each cycle of the pulse generator produces two data inputs, one High and one Low. A pulse generator operating at 5MHz produces an input data rate of 10MHz.

As an example using the 74F5074, assume that one failure per century is acceptable and both data and the clock are at 10MHz. A typical tau for the 54F5074 is 135 picoseconds with a T_0 of 9.8E6 seconds. Since one century equals about three billion seconds, substituting into the equation above gives:

$$3E9\ \text{sec} = \frac{\left[\exp\left(\frac{t'}{0.135ns}\right)\right]}{[9.8E6(10MHz)\ (10MHz)]}$$

$$t' = 9.5ns$$

If an additional nanosecond were allowed between the clock and the sampling point, one could expect a failure about once every 1.7 million years.

The 74F728 MTBF can be determined by setting the clock period to the t′ so that in the example above the t′ = 100ns. This t′ gives:

$$MTBF = \frac{\left[\exp\left(\frac{100ns}{0.135ns}\right)\right]}{[9.8E6(10MHz)\ (10MHz)]}$$

MTBF = 5.0E321 seconds
or 1.6E312 centuries!

Note that in this case a failure is considered to be any propagation delay beyond the delay expected in a situation where setup and hold times were not violated. Assuming data and clock rates of 100MHz gives:

$$MTBF = \frac{\left[\exp\left(\frac{10ns}{0.135ns}\right)\right]}{[9.8E6(100MHz)\ (100MHz)]}$$

MTBF = 1.5E9 seconds
or 48 years!

SKEW CHARACTERISTICS

One of the requirements for an effective clock driver is that the complementary outputs have a small skew relative to each other. Figure 5 shows a picture of the 74F5074 outputs at room temperature with a 5 volt V_{CC}. Because of Philips Semiconductors patented circuitry the output skews will always remain tightly coupled over temperature and V_{CC}.

SUMMARY

Because of their minimum output skews, metastable immune characteristics, and balanced output drive capabilities, the 74F50XXX series of products offer viable solutions to synchronization and clock driver problems.

For further reading on the metastability problem, Philips Semiconductors recommends Application Note AN219, “A Metastability Primer”, and “Metastability Behavior in Digital Systems” by Lindsay Kleeman and Antonio Cantoni in *IEEE Design & Test of Computers*, December 1987, pages 4–19.

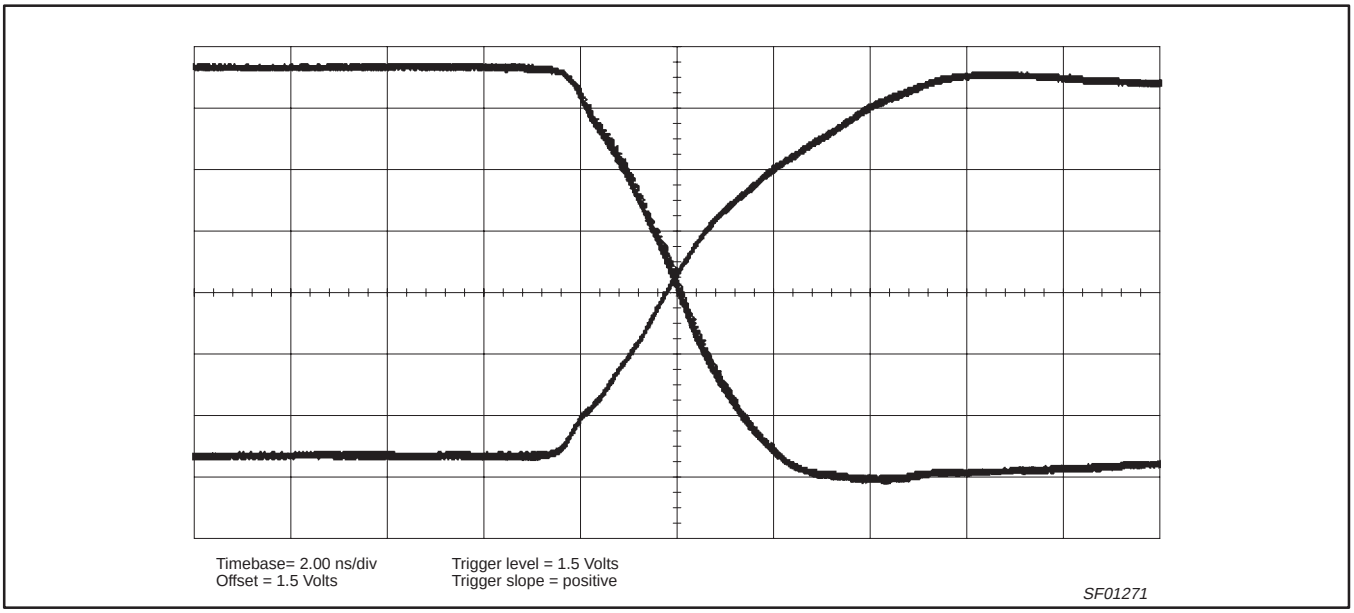

Figure 5. 74F5074 $\overline{Q}$ and Q Outputs Skew Relationship at 5 Volts V_{CC} and Room Temperature

NOTES

Synchronizing and clock driving solutions – using the 74F50XXX family

AN220

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

Let's make things better.

Philips Semiconductors

PHILIPS